REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has made a minor amendment to the form of claim 1, not related to patentability of the claimed subject matter. Accordingly, claims 1, 2, 4-12, 14-18 and 20-23 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Claim Rejections – 35 U.S.C. § 102(b)

On Page 2 of the Office Action, the Examiner rejected claims 1-2, 4-5, 7-12, 14, 17-18, 20-21 and 23 under 35 U.S.C. § 102(b) as being anticipated by Chatterjee, et al. (US 5,634,046, hereinafter referred to as Chatterjee). The Applicant respectfully traverses this rejection.

It is important to remember that anticipation requires that the disclosure of a single piece of prior art reveals every element, or limitation, of a claimed invention. Furthermore, the limitation that must be met by an anticipatory reference are those set forth in each statement of function in a claims limitation, and such a limitation cannot be met by an element in a reference that performs a different function, even though it may be part of a device embodying the same general overall concept. Chatterjee fails to anticipate each and every limitation of claim 1. Therefore, claim 1 is not anticipated.

Claim 1 recites:

1. A computer system comprising:

a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory address calculation information received from memory, said special-purpose register file having at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to said special-purpose register file;

wherein said at least one dedicated interface includes a dedicated direct path between said special-purpose register file and memory for loading said special-purpose access register file from memory;

means for determining a memory address in response to memory address calculation information received from said special-purpose register file, thus enabling a corresponding memory access. (emphasis added).

The Applicant's invention provides a dedicated direct path between the memory and the special-purpose register to allow transfer of memory address calculation in parallel with other data being transferred to and/or from the general register files. Claim 1 also recites a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory address calculation information received from memory (see page 4, lines 15-24; page 7, lines 26-30 of the Applicant's specification). The Applicant's claimed invention provides a special-purpose register file which is dedicated for storing memory address calculations. This special-purpose register file is separate from other general register files. By separating (in terms of functionality) the special-purpose register files from other files, the present invention provides effective and efficient memory access by the computer not shown in any prior art.

In contrast to the Applicant's invention, Chatterjee discloses a stack pointer register in a computer having a register set 18 holding both general and special registers interfacing with a main memory 14 through a single bus 16. The Examiner stated that Chatterjee discloses a dedicated special-purpose register file 18 comprising CS 38, SS 39, DS 40, ES 41, FS 42, and GS 43. The Examiner cites the bus 16 as providing a dedicated interface between the special-purpose register for allowing efficient transfer of memory address calculation information in relation to the special-purpose register file. The Applicant respectfully disagrees with this characterization. Although the register file 18 does disclose the register file 18 containing CS 38, SS 39, DS 40, ES 41, FS 42, and GS 43, this register file 18 also contains the general registers 30-37 (see Col. 4, lines 41-52; FIGs. 1 and 2 of Chatterjee). Chatterjee clearly states that the register set includes both special-purpose and general registers. Thus, the bus 16 provides a single interface to both the special-purpose and general registers. The communication between the CS register and the main memory must go through the single bus interface 16, which provides a path to both the special-purpose and general registers.

Thus, Chatterjee fails to disclose one dedicated interface having a dedicated direct path between the special-purpose register file and memory for loading the special-purpose access register file from memory. Therefore, Chatterjee does not

anticipate claim 1. Similarly, claim 17 contains limitations analagous to claim 1. Therfore, claim 17 is also not anticipated by Chatterjee. Claims 2, 4-5, 7-12, 14, and 23 depend from claim 1 and recite further limitations in combination with the novel elements of claim 1. Claims 18, 20, and 21 depend from claim 17 and recite further limitations in combination with the novel elements of claim 17. Therefore, the allowance of claims 1-2, 4-5, 7-12, 14, 17-18, 20-21 and 23 is respectfully requested.

3.) Claim Rejections – 35 U.S.C. § 103(a)

On Page 23 of the Office Action, the Examiner rejected claims 6, 15-16 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee in view of Aikawa et al. (US 5,371,865, hereinafter referred to as Aikawa). The Applicant respectfully traverses this rejection.

As stated above, Chatterjee fails to disclose one dedicated interface having a dedicated direct path between the special-purpose register file and memory for loading the special-purpose access register file from memory. In fact, Chatterjee clearly teaches a register set that includes both special-purpose and general registers. Thus, Chatterjee does not contain all the elements recited in claims 1 and 17 and even teaches away from a special-purpose register file. The addition of Aikawa does not make up the missing elements. In addition, rejected claim 15 contains limitations analagous to claims 1 and 17. Therfore, the combination of Chattejee and Aikawa does not teach or suggest all the elements recited in independent claims 1, 15, and 17. Claim 6 depends from claim 1 and recites further limitations in combination with the novel elements of claim 1. Claim 16 depends from claim 15 and recites further limitations in combination with the novel elements of claim 15. Claim 22 depends from claim 17 and recites further limitations in combination with the novel elements of claim 17. Therefore, the allowance of claims 6, 15, 16, and 22 is respectfully requested.

4.) Prior Art Not Relied Upon

On Page 34 of the Office Action, the Examiner stated that the prior art made of record and not relied upon is considered pertinent to the Applicant's invention. A reading of these references, however, has not revealed any teaching or suggestion of a

computer system having a dedicated special-purpose register file separate from other general register files of the computer system, at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to the special-purpose register file, wherein the dedicated interface includes a dedicated direct path between the special-purpose register file and memory for loading the special-purpose access register file from memory.

5.) Conclusion

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 1, 2, 4-12, 14-18 and 20-23.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would expedite the prosecution of the Application.

Respectfully submitted,

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